LATENCY TEST OF ENERGY STORAGE SYSTEM (ESS)

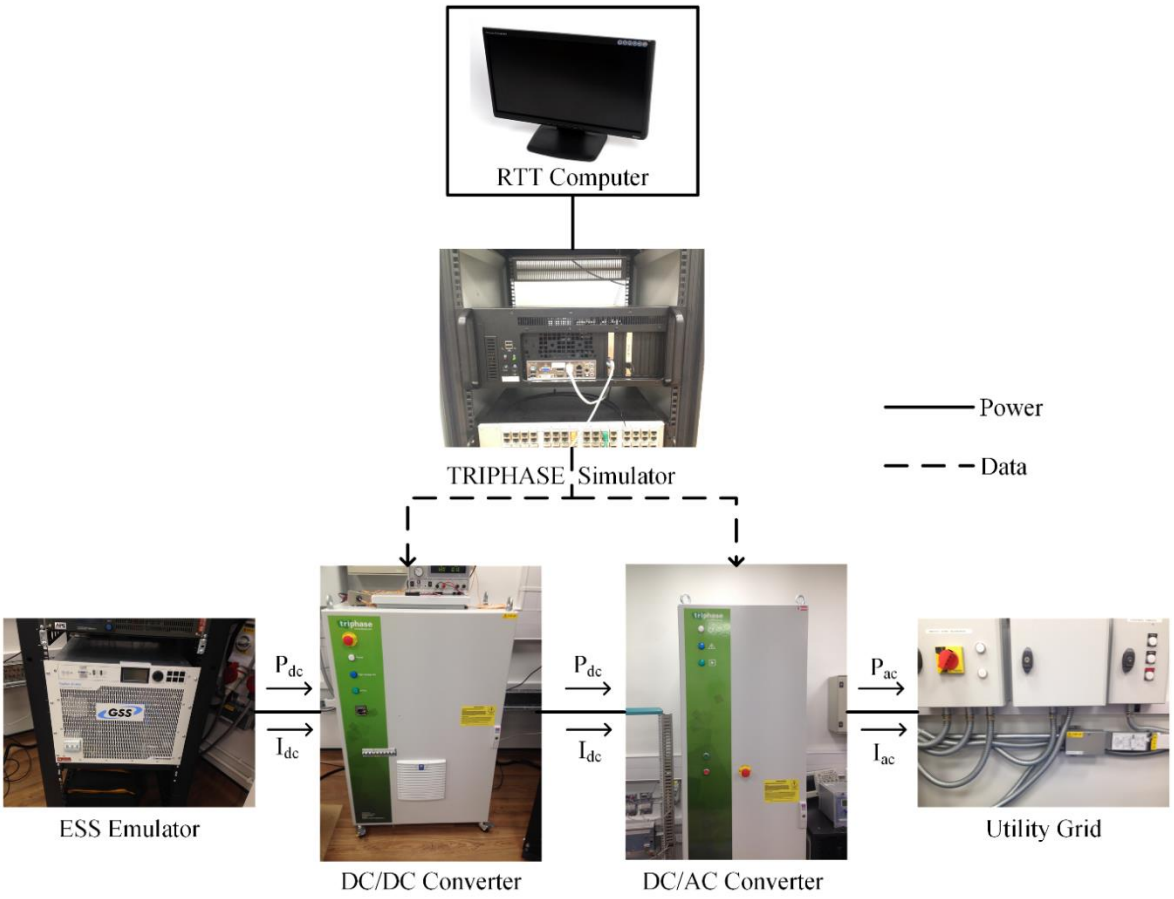


Figure 1: Experimental ESS Test Bed

1. Brief description of ESS Test Bed

An illustration of the laboratory set up, to conduct the experiments for estimating the response time of the ESS, is shown in Figure 1. The Smart Grid Laboratory at Newcastle University where this experiment took place, is designed to synergistically combine the scale of simulation with the detail of experimentation. This is achieved through Flexible Power Conversion Systems (FPCSs), real and emulated ESS, and real-time simulation. For the purposes of this experiment, as shown in Fig. 1, an ESS emulator is coupled to a 415 V busbar of the laboratory network through a DC/ DC power converter and a DC/AC power converter.

In the experiments presented here, an ESS emulator is used to represent a Li-Ion battery. The emulator is programmed with the characteristics of a Li-Ion battery, with a single string of 50 series cells, each with a nominal voltage of 4 V & a capacity of 200 Ah; these parameters are selected in order to set the nominal voltage, power and energy ratings of the ESS as 200 V, 20 kW and 40 kWh respectively.

Real-time simulation is carried out using a TRIPHASE real-time simulator to model the ESS network. This technology enables ESS models to be run in real-time, and allows the laboratory hardware to operate as though it is coupled to a real distribution-scale network. The controllers for DC/DC and DC/AC converters are implemented as MATLAB Simulink models, embedded within the TRIPHASE Simulator.

2. Key Definitions

Communication Latency t_2: It is defined as the time taken by the DC current I_{dc} or DC power P_{dc} to reach the steady-state reference value, after the command signal is sent at time instant t_1 by the TRIPHASE simulator to the controller of DC/DC converter.

Communication Latency t_3: This is the time span from the time instant t_1 and the time instant at which the AC output current of DC/AC converter reaches steady state value.

Communication Latency t_4: This is the time duration from the time instant t_1 and the time instant at which the AC output power of the DC/AC converter reaches the steady-state value. This time is same as the total response time t_{resp}.

$$t_{resp} = t_4$$

3. Tests to estimate the response time of ESS

Power reference command signals are sent using the MATLAB Simulink controllers of both the converters. The different voltage, current and power variables of the system are recorded and stored using a tool called Data Logger used in the Simulink model. From these data, the communication latency durations are estimated, and the total response time is calculated. Basically, three rounds of real power (P) tests are to be conducted with different power levels as shown below:

- 33% of the nominal kW rating, i.e. 6.6 kW
- 66% of the nominal kW rating, i.e. 13.2 kW
- 100% of the nominal kW rating, i.e. 20 kW (Rated Current = 100 A)

For 33% rating, the tests include 6 step tests in sequential order as given below:

- 0% step up to +33% of the P set level
- +33% step down to 0% of the P set level
- 0% step down to -33% of the P set level

- -33% reverse to +33% of the P set level
- 33% reverse to -33% of the P set level
- -33% step up to 0% of the P set level

Similarly, these tests are conducted for 66% and 100% of the nominal kW rating. In the given test, the nominal power rating of the ESS is fixed at 20 kW. A sample test result for the first round, i.e., 0% step up to +33% of the nominal P level, is shown below in Figure 2 to clearly illustrate the how the different communication latencies namely t_2, t_3 and t_4 are measured. The time durations namely t_2, t_3 and t_4 are thus measured in parallel from the instant t_1 as shown in Fig. 2. The AC & DC current signals shown in Fig. 2 corresponds to Table 1. Also, four different battery SoC levels, 25%, 45%, 65%, and 85% are selected to conduct the tests. The results in tables 2 and 3 are obtained in a similar way as in Table 1. The data file provided along with this document corresponds to Table 1 only. The DC & AC current waveforms, corresponding to Fig. 2, are provided in the Appendix section.

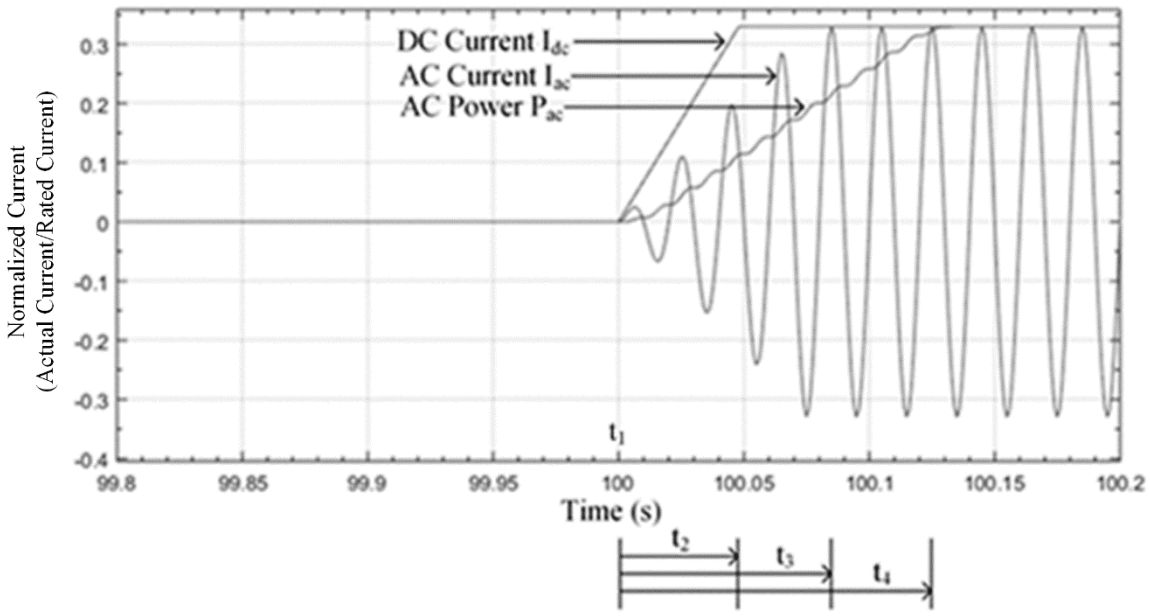


Figure 2: Time latencies for 0% to 33% step change in nominal real power rating of ESS Emulator

4. Results of ESS

The real power tests as explained in the previous sub-section are conducted and the following results are tabulated and summarized. The total and average response times for each case are also calculated.

Table 1: Real Power Test at 33% of the nominal kW rating

P Command	0 to 1/3	1/3 to 0	0 to -1/3	-1/3 to 1/3	1/3 to -1/3	-1/3 to 0	Average
t_2 (ms)	50	48	51	45	56	49	49.8
t_3 (ms)	85	81	79	80	77	88	81.6
t_4 (ms) (t_{resp} (ms))	125	117	127	134	137	141	130.1

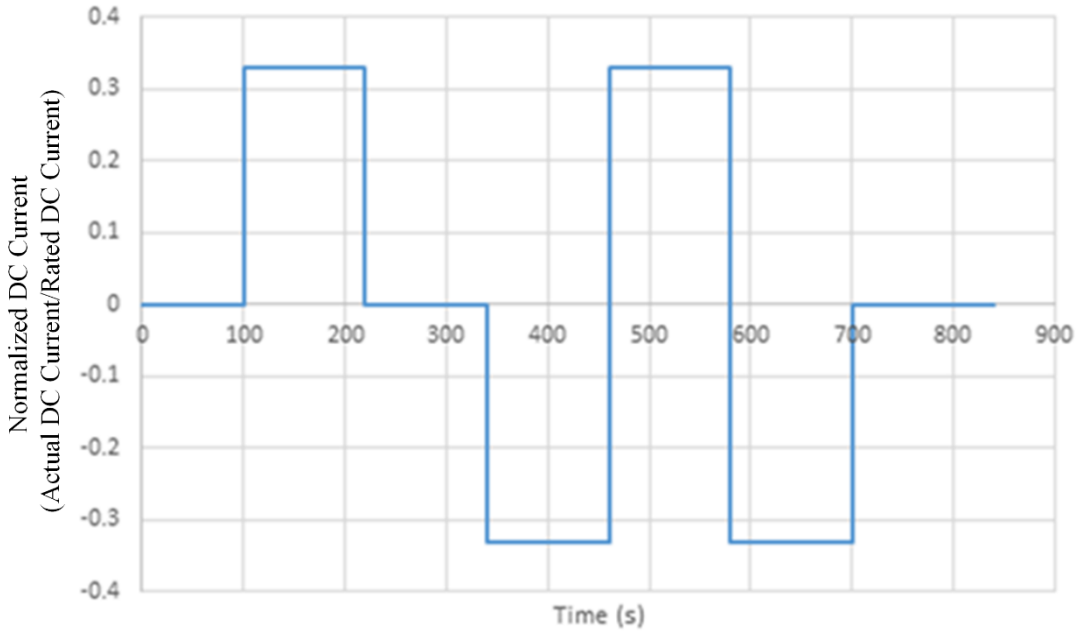
Table 2: Real Power Test at 66% of the nominal kW rating

P Command	0 to 2/3	2/3 to 0	0 to -2/3	-2/3 to 2/3	2/3 to -2/3	-2/3 to 0	Average
t_2 (ms)	45	50	55	61	59	63	55.5
t_3 (ms)	75	83	79	88	82	76	81
t_4 (ms) (t_{resp} (ms))	129	135	131	131	140	138	134

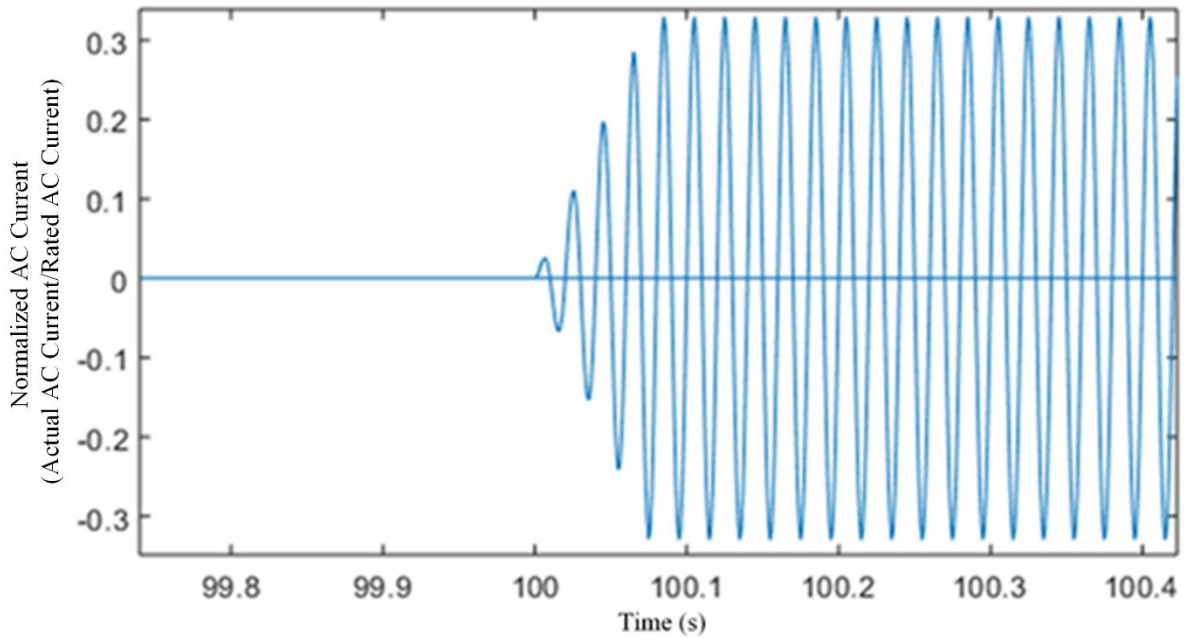
Table 3: Real Power Test at 100% of the nominal kW rating

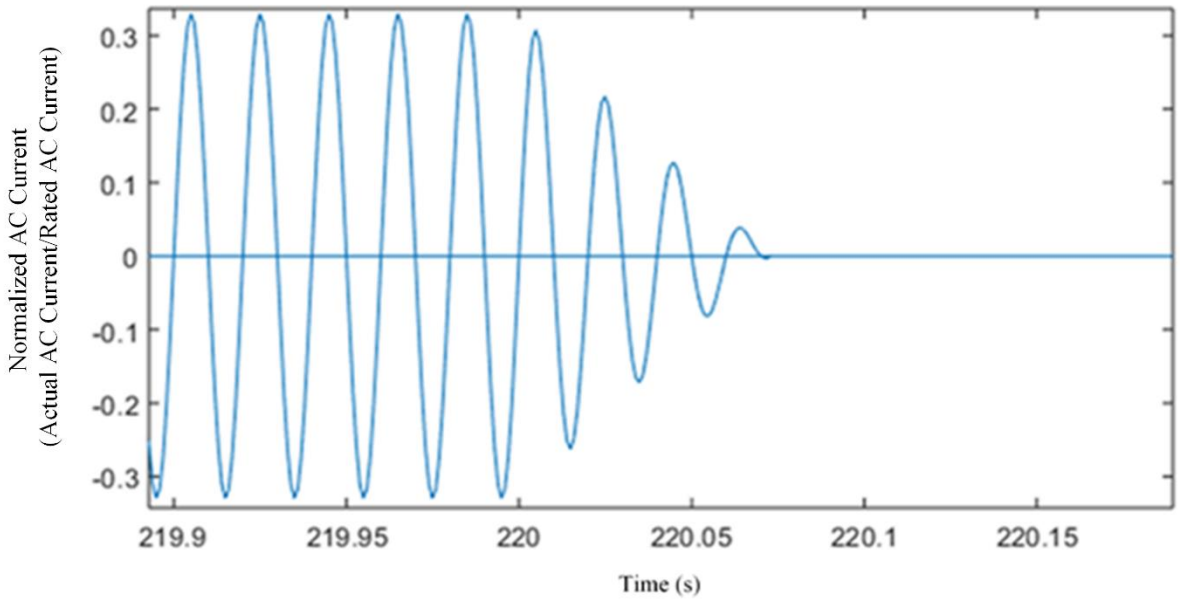
P Command	0 to 1	1 to 0	0 to -1	-1 to 1	1 to -1	-1 to 0	Average
t_2 (ms)	55	59	52	60	57	48	55.16
t_3 (ms)	88	72	84	86	91	87	82.16
t_4 (ms) (t_{resp} (ms))	117	111	126	115	122	133	121.3

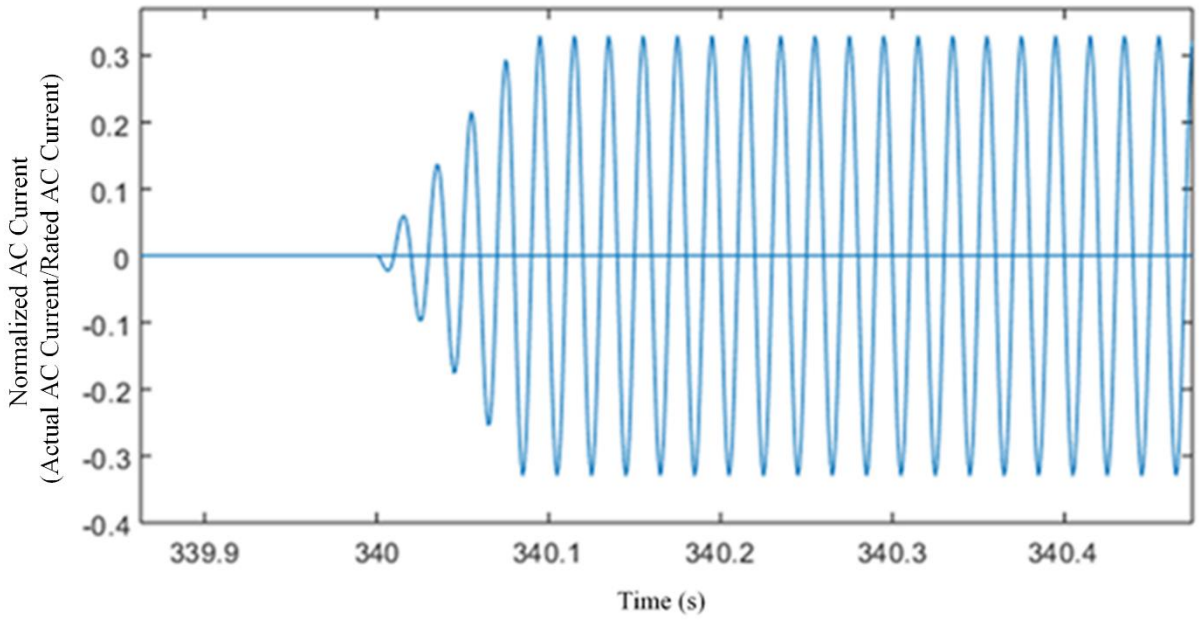
Appendix

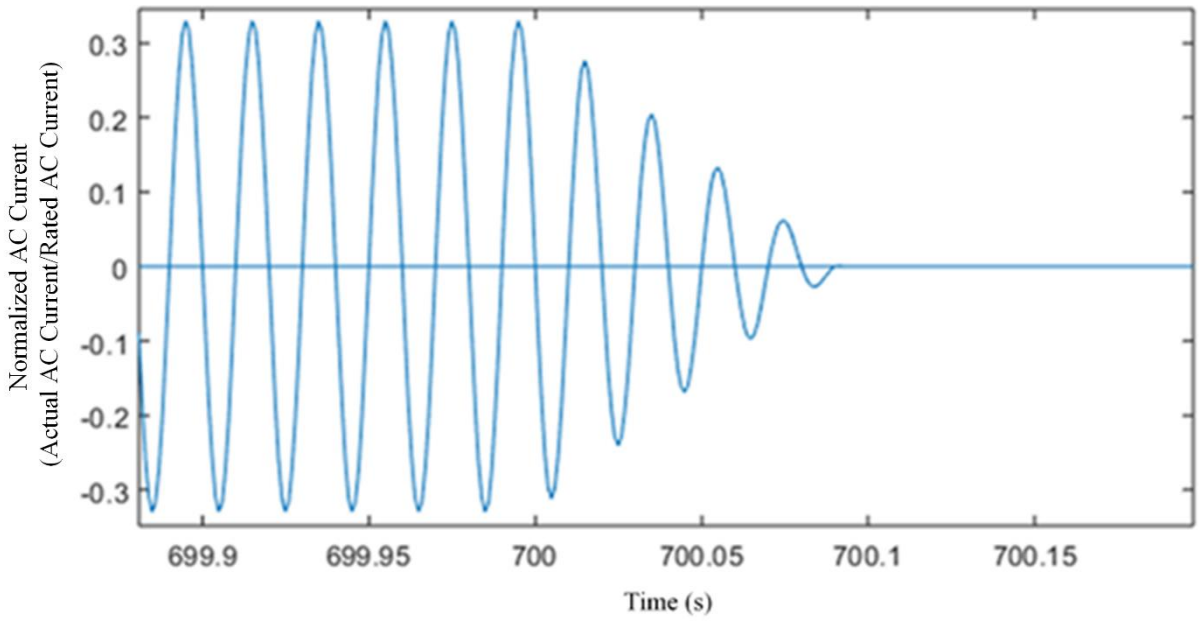


Zoomed-in AC Waveforms




Normalized AC Current
(Actual AC Current/Rated AC Current)
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
219.9
219.95
220
220.05
220.1
220.15
Time (s)


Normalized AC Current
(Actual AC Current/Rated AC Current)
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
-0.4
339.9
340
340.1
340.2
340.3
340.4
Time (s)


Normalized AC Current
(Actual AC Current/Rated AC Current)
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
699.9
699.95
700
700.05
700.1
700.15
Time (s)